

Claims

- 1 1. A logic simulation hardware emulator, comprising:

2 a simulation model comprising one or more source emulation processors
3 coupled to one or more receiving emulation processors by an emulation
4 cable having a plurality of signal wires, the plurality of signal wires
5 comprising a plurality of regular signal wires and one or more spare signal
6 wires; and

7 a runtime control program for controlling the simulation model, wherein
8 upon detection of a fault on a regular signal wire, the runtime control
9 program reassigns a signal on the regular signal wire having the fault to
10 the one or more spare signal wires.
- 1 2. The logic simulation hardware emulator of claim 1, wherein the one or more
2 spare signal wires are defined at simulation model build time.
- 1 3. The logic simulation hardware emulator of claim 3, wherein the one or more
2 spare signal wires are defined by designating one or more emulation processors
3 and their corresponding regular signal wires as faulty during simulation model
4 build.
- 1 4. The logic simulation hardware emulator of claim 1, wherein the logic simulation
2 hardware emulator further comprises a spare select multiplexer, the inputs of the
3 spare select multiplexer coupled to the outputs of the one or more source
4 emulation processors, and output of the spare select multiplexer coupled to the
5 input of the emulation cable, wherein the spare select multiplexer multiplexes the
6 signal on the regular signal wire having the fault through the one or more spare
7 signal wires.
- 1 5. The logic simulation hardware emulator of claim 4, wherein a signal select for the
2 spare select multiplexer is provided by a spare select register.

- 1 6. The logic simulation hardware emulator of claim 5, wherein the spare select
2 register is updated by the runtime control program during the simulation run.
- 1 7. The logic simulation hardware emulator of claim 1, wherein the simulation
2 hardware emulator further comprises:
- 3 one or more source type multiplexers coupled to an output of the emulation
4 cable, wherein each of the source type multiplexers has a select signal; and
- 5 a plurality of processor selector multiplexers coupled to the outputs of the one or
6 more source type multiplexers, wherein the output of each processor selector
7 multiplexer is coupled to an input of one or more receiving emulation processors,
8 and wherein each of the processor selector multiplexers has a select signal.
- 1 8. The logic simulation hardware emulator of claim 7, wherein the select signals for
2 the source type multiplexer and the processor selector multiplexer are provided
3 by the runtime control program.

- 1 9. A method for the automatic reconfiguration of faulty signal wires in a logic
2 simulation hardware emulator, the logic simulation hardware emulator having one
3 or more source emulation processors coupled to one or more receiving emulation
4 processors by a set of emulation cables, each emulation cable having a plurality
5 of signal wires; the plurality of signal wires comprising a plurality of regular signal
6 wires and one or more predefined spare signal wires, the method comprising the
7 steps of:

8 identifying a set of faulty signal wires within the plurality of regular signal
9 wires, if any faulty signal wires exist; and

10 reassigning signals from the set of faulty signal wires to the one or more
11 spare signal wires within the set of emulation cables.
- 1 10. The method of claim 9, wherein the method further includes the step of:

2 performing a connectivity diagnostic on the set of emulation cables within
3 the hardware emulator.
- 1 11. The method of claim 9, wherein the method further includes the step of:

2 predefining one or more spare signal wires within the emulation cables at
3 simulation model build time.
- 1 12. The method of claim 9, wherein the step of reassigning signals from the set of
2 faulty signal wires to one or more spare signal wires within the set of emulation
3 cables includes the steps of:

4 determining if a spare signal wire is available, if one or more faulty signal
5 wires exist;

6 setting a source module spare register to a value corresponding to the
7 source emulation processor having the faulty wire; and

- 8 changing any receiving emulation processor steps sourced by the faulty
- 9 wire to the spare wire.

1 13. A computer-readable program stored on a computer-readable medium, the
 2 computer readable program providing the automatic reconfiguration of faulty
 3 signal wires in a logic simulation hardware emulator, the logic simulation
 4 hardware emulator having one or more source emulation processors coupled to
 5 a one or more receiving emulation processors by a set of emulation cables, each
 6 emulation cable having a plurality of signal wires; the plurality of signal wires
 7 comprising a plurality of regular signal wires and one or more predefined spare
 8 signal wires, the computer readable program being configured to perform the
 9 steps of:

10 identifying a set of faulty signal wires within the plurality of regular signal
 11 wires, if any faulty signals wires exist; and

12 reassigning signals from the set of faulty signal wires to the one or more
 13 spare signal wires within the set of emulation cables.

1 14. The computer-readable program of claim 13, wherein the computer-readable
 2 program further includes the step of:

3 performing a connectivity diagnostic on the set of emulation cables within
 4 the hardware emulator.

1 15. The computer-readable program of claim 13, wherein the method further includes
 2 the step of:

3 predefining one or more spare signal wires within the emulation cables at
 4 simulation model build time.

- 1 16. The computer-readable program of claim 13, wherein the step of reassigning
2 signals from the set of faulty signal wires to one or more spare signal wires within
3 the set of emulation cables includes the steps of:
- 4 determining if a spare signal wire is available, if one or more faulty signal
5 wires exist;
- 6 setting a source module spare register to a value corresponding to the
7 source emulation processor having the faulty wire; and
- 8 changing any receiving emulation processor steps sourced by the faulty
9 wire to the spare wire.